PATENT TECHNOLOGY FOR

SPEEDING EXECUTION OF SOFTWARE CODE

&

RESOURCE OPTIMIZATION

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DETAILS OF THE REGISTERED PATENTS:

US 8,949,786

Method and System for Parallelization of Sequential Computer Program Codes /Method for speeding execution of computer programs

Inventors : Dr. Vaidya, Priti Ranadive and Sudhakar Sah

US 8,732,714

Method for Reorganizing Tasks for Optimization of Resources

Inventor : Dr. Vaidya, Priti Ranadive, Sudhakar Sah and Jaydeep Vipradas

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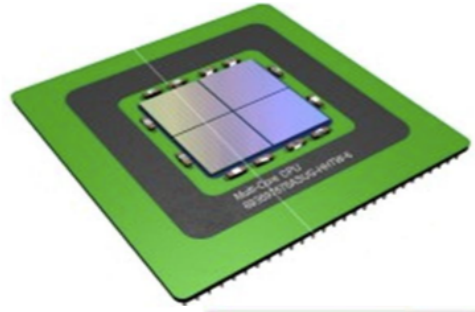
METHOD AND SYSTEM FOR SPEEDING EXECUTION OF SOFTWARE CODE

Challenges :

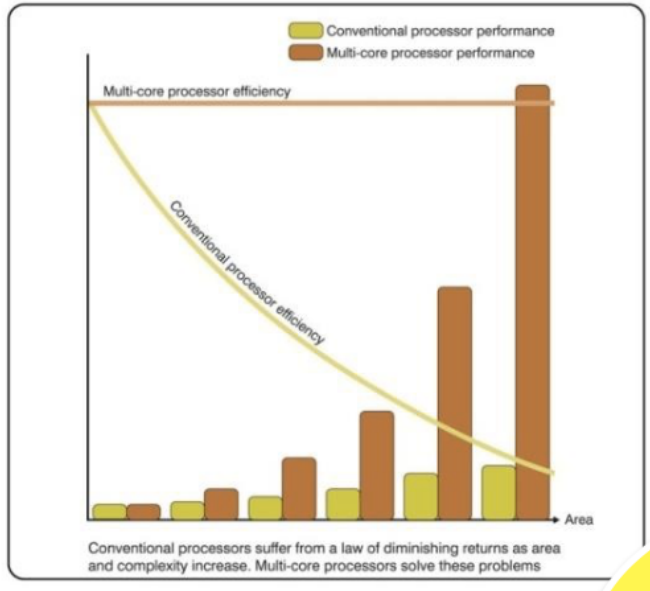
Multicore processors have taken over the market, but software applications written are sequential in nature. To fully exploit multicore processors, there is a need to convert sequential code to concurrent code.

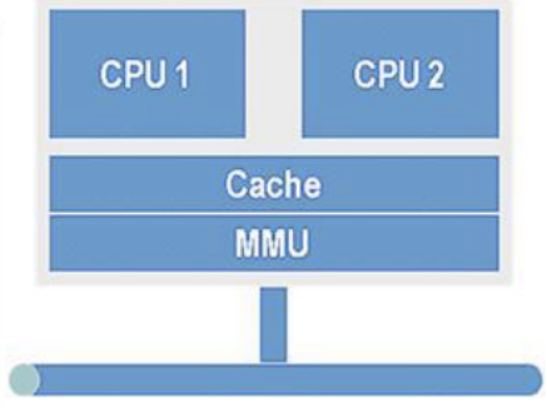


Our Solution:

We have developed a method and a tool that:

- Converts legacy software code to parallel code automatically.
- Requires no manual intervention.
- Requires no re-writing of application.
- Executes the code faster.
- Assists the user in identifying the optimal number of processor cores required for the application to be executed in parallel.
- Allows output parallel code in standard OpenMP/MPI or user specific format.
- Addresses all types of code segments - as opposed to currently available tools that parallelize only loops or specific applications that are embarrassingly parallel.





Areas of Application
Embedded systems, automotive systems, parallel systems, Networking, Manufacturing, automation

KEY CLAIMED STEPS FOR IMPLEMENTATION OF US 8,949,7866 PATENT

METHOD OF REORGANIZING TASKS TO ACHIEVE RESOURCE OPTIMIZATION

Challenges :

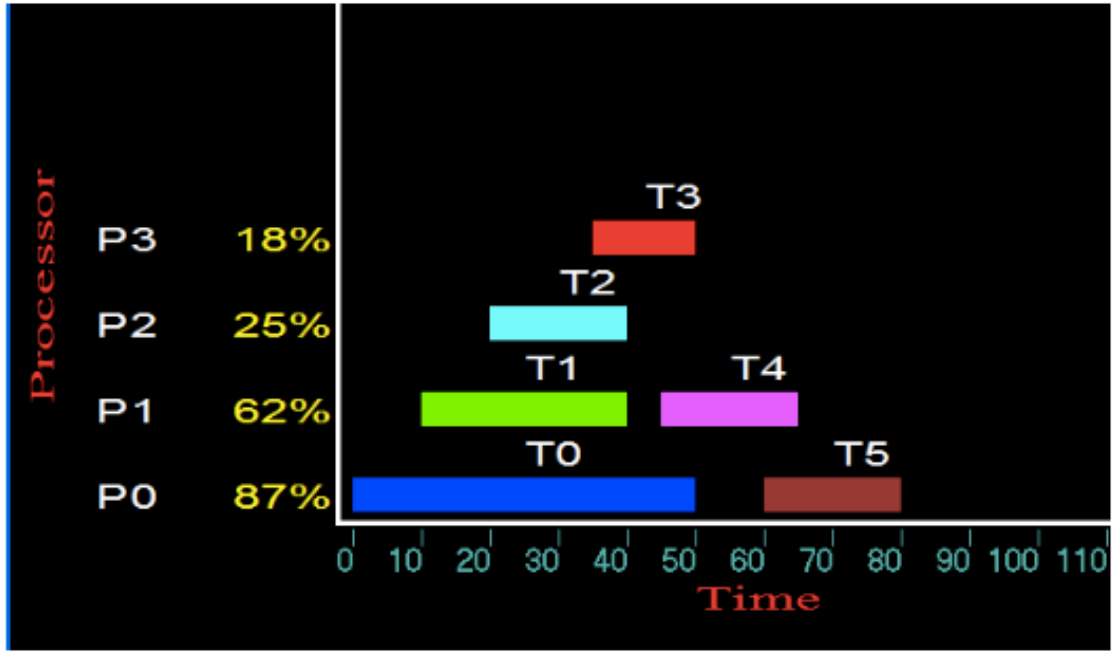
Parallelizable code segments and their dependencies are identified, but to exploit available multicore or parallel systems, a good scheduling policy is required.

Our Solution:

We have invented a method that:

- Assists user in identifying the optimized number of cores/processors required for the given number of tasks to be executed in parallel.
- Static scheduler - Gives a detailed schedule with start time, wait time and end time of each tasks.
- Dynamic scheduler – Processors/cores indicate their availability, and tasks are given priority based on dependencies. No master-slave relation.
- Design scalable to any number of processors/cores.
- Design and method applicable to both AMPs and SMPs (Homogenous and heterogeneous cores/processors).
- Parts of method applicable to any other processes e.g. manufacturing process.

Areas of Application
Embedded systems
Automotive systems
High Performance Computing
Parallel systems
Networking
Manufacturing



KEY CLAIMED STEPS FOR IMPLEMENTATION OF US 8,732,714 PATENT

Mapping each of a plurality of tasks to determine data indicative of dependencies for each task, to identify any releasing tasks on which depends a respective task based on the dependencies indicative data, to make the respective task wait until after the releasing task begins execution before the respective task can begin execution, and to allow elapse of an offset time after the releasing task begins execution before the respective task may begin execution

Generating a matrix having a row and a column for each of the plurality of tasks and a plurality of matrix data elements, each of which are associated with a first task and a second task of the plurality of tasks, and allowing an elapse of an offset time after the first task begins execution before the second task may begin execution

Reorganizing the plurality of tasks in accordance with the plurality of matrix data elements

IP SNAPSHOT

Patent Title/Description	Domain	Country	Application/Patent Number	Patent Status
Method and System for Parallelization of Sequential Computer Program Codes /Method for speeding execution of computer programs	High Performance Computing	PCT	PCT/IN2009/000697	Completed
		U.S.	US 8,949,786	Granted
			US 14/606,924	In Prosecution
		Japan	JP2012510661	In Prosecution
			JP 2015-154050 (divisional)	In Prosecution
Method for Reorganizing Tasks for Optimization of Resources	High Performance Computing	India	2559/MUM/2008	In Prosecution
		PCT	PCT/IN2009/000701	Completed
		Europe	EP2356567	In Prosecution
		U.S.	US 8,732,714	Granted
		Japan	JP2012511204	Dropped

EXPECTATIONS:

- Company seeks alliance with Potential Licensees to assign Licensing Rights to Market these technologies.

- Company is also interested in sale of the Granted/Issued Patents.

THANK YOU