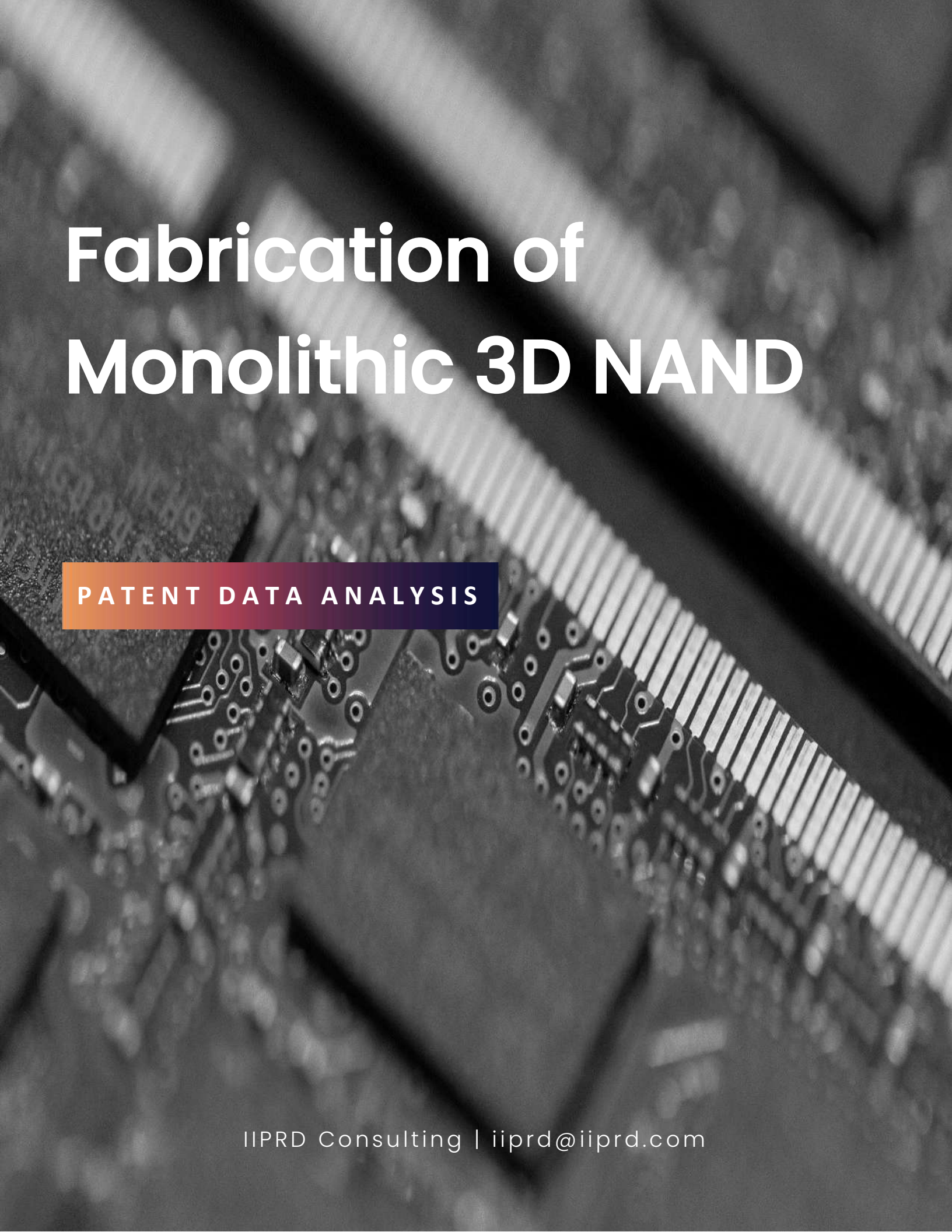

Fabrication of Monolithic 3D NAND

PATENT DATA ANALYSIS

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SUMMARY

Competition in NAND Flash Market is set to intensify in 2022 considering the recent developments in 5G space and IoT. A major challenge before memory manufacturers is to increase the memory capacity without foregoing memory size. Thus, 3D NAND memories, more specifically monolithic 3D NAND memories due to high areal density, are expected to play a major role in the coming years.

In this report, we study the Intellectual Property (Patents) landscape of this fast-growing technology. An analysis of worldwide patents related to the fabrication of Monolithic 3D NAND memory published after Jan 2018 shows that China's Yangtze Memory Technologies ("YMTC") is leading the race with its propriety Xtacking™ technology. YMTC gave a clear hint about this in 2020 when it unveiled 128 Layer 3D NAND memory. Western Digital/ SanDisk® and KIOXIA Group, two of the 'big four' memory fabricators are gearing up in this space and are actively investing in R&D to scale up the efficiency and yield of fabrication techniques. While industry leader Samsung Electronics is ready to give tough competition to the Western Digital & KIOXIA team. On the other hand, it seems companies like SK Hynix (which also includes Intel Corporation), and Micron Technology needs a better technology plan to compete in this space.

INTRODUCTION

WHAT IS SSD?

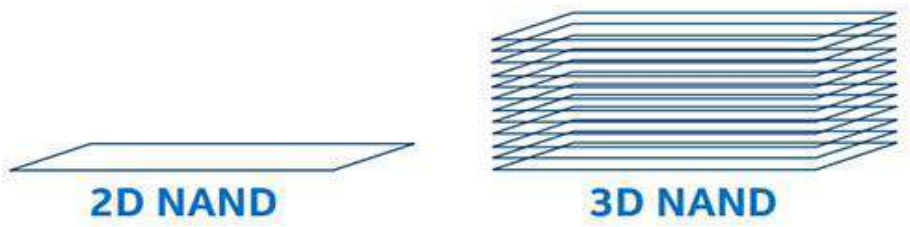
NAND Flash originally hit the market in 1991 with a 4Mb product by Toshiba (now Kioxia), and after continuous growth and scaling, NAND has become the topmost choice for non-volatile storage technology with Tb-class density and annual revenues over $55 billion (2020) for majority of consumer electronic device manufacturers.

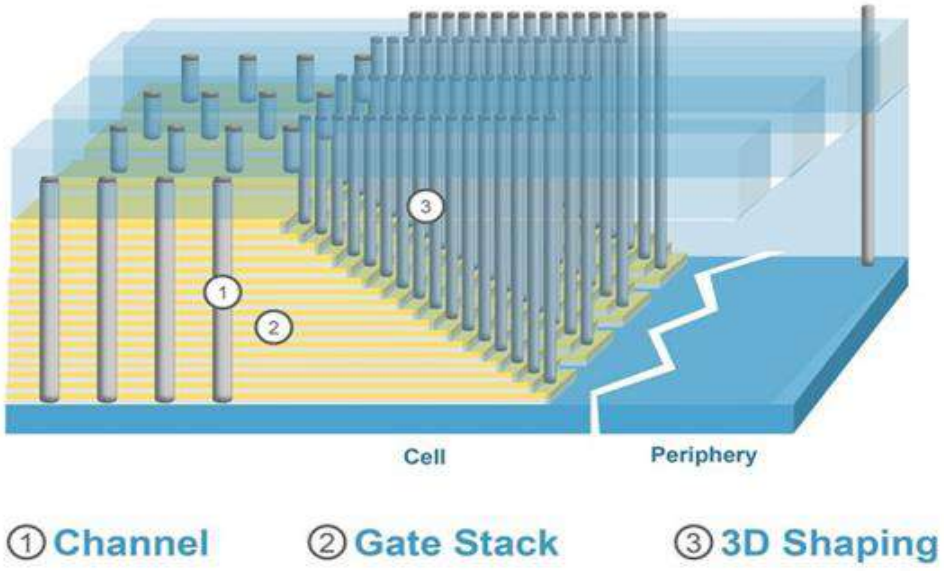
A typical NAND memory cell involves a transistor structure with a control gate and a floating gate where electrons are stored and removed from the floating gate by applying a voltage to the cell.

2D SSD AND 3D SSD

In the last decade, due to surge in IoT based systems, connected vehicles, smart devices and 5G technology, the adoption of NAND has hit the top gear. For years, the industry used planar 2D NAND technology where a series of memory cells are connected in series along a horizontal string which consumes lot of space in a consumer electronic device. Growing market interest in mini and micro devices has led to growth in demand of high-capacity memory in the last decade, as a result, industry has seen a major technological transition from planar 2D to 3D architectures with continuous scaling through vertical stacking of memory cells.

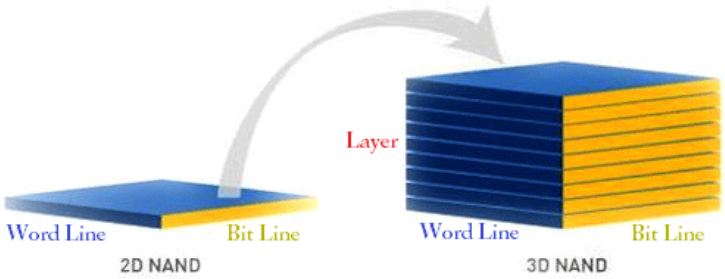
In 3D NAND, the memory cell string is stretched, folded over and stacked vertically (often referred to as V-NAND by Samsung). The cells are stacked vertically thus leaving a scope to scale the density and capacity of NAND memory.





Source

In a 3D NAND, layers describe the number of wordlines that are stacked up on top of each other and a vertical pillar is cut through those wordline layers. Intersection of that pillar with each of those wordlines represents a single physical cell. Each 3D NAND cell consists of a vertical channel in the middle, followed by a charge layer inside the structure.



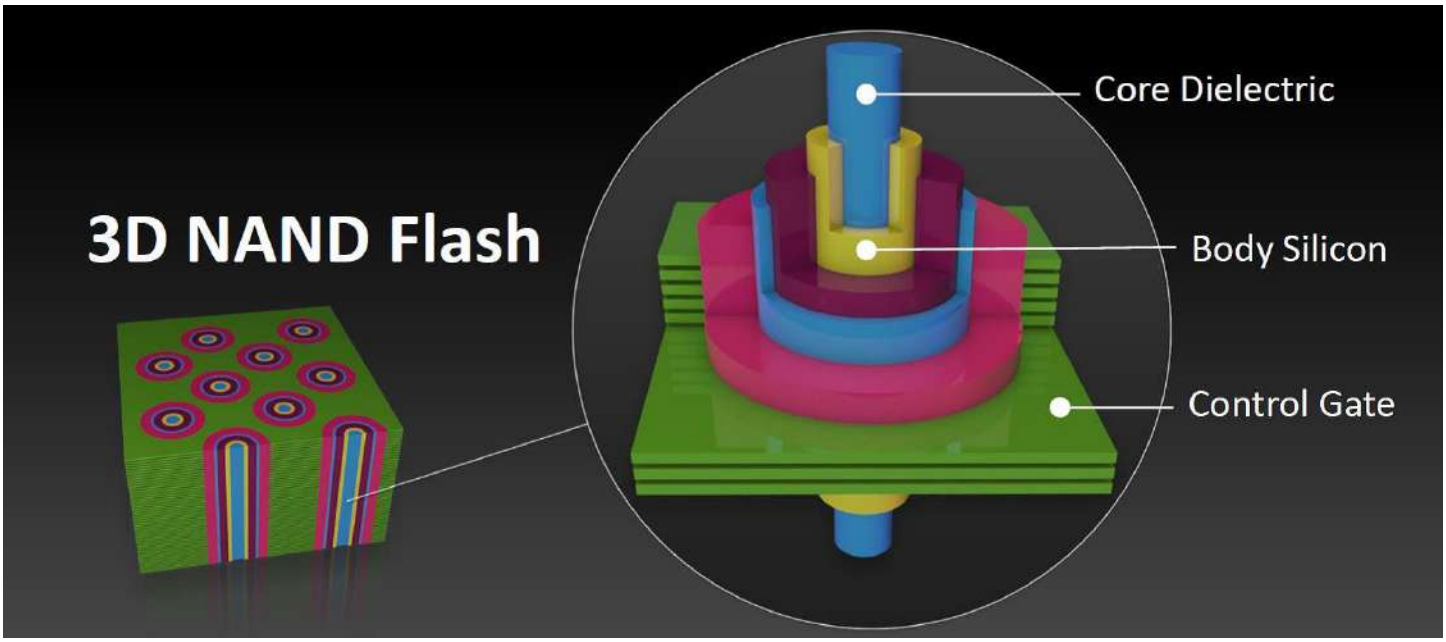


Image source: SanDisk

MONOLITHIC 3D NAND

Why 3D NAND?

- Restricted Scaling
- Increased Areal Density

Patenting since Jan 2018

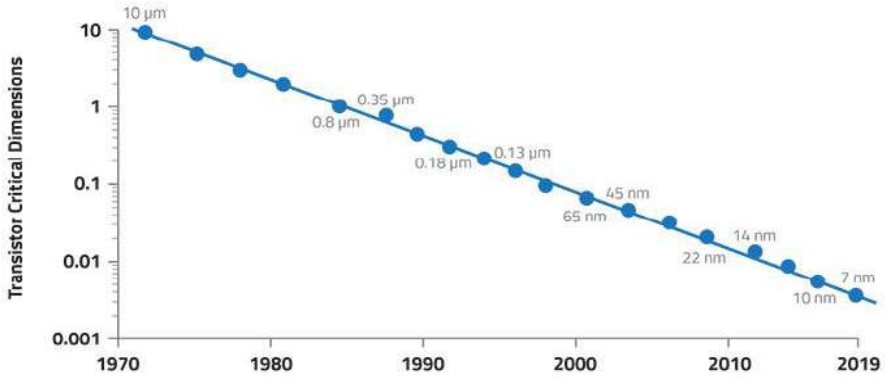
- Key technology holders
- Upcoming patents

Pace of Innovation

- Speedy grant of patents
- YMTC and its path and future

WHY 3D NAND?

Over the past few years, cell size of planar NAND has been scaled from 120nm to the 14 nm node, thus enabling 100 times more storage capacity. But now, the technology can no longer scale.

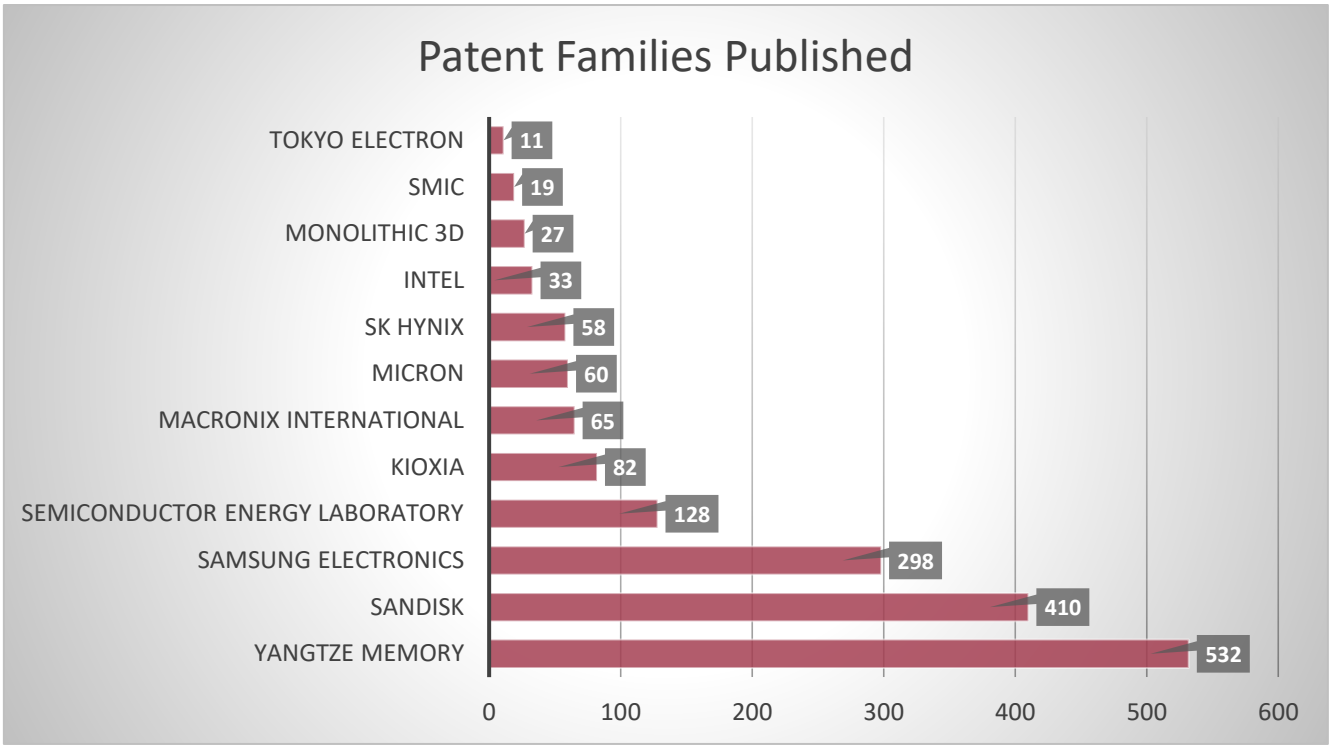


That's where 3D NAND comes into picture. Typically, memory cell density increases directly with the number of layers in the stack and thus there is a race to stack more layers onto a substrate. Most memory manufacturers are currently fabricating 64- and 96-layer technology, which enables 256-Gbit and 512-Gbit 3D NAND devices.

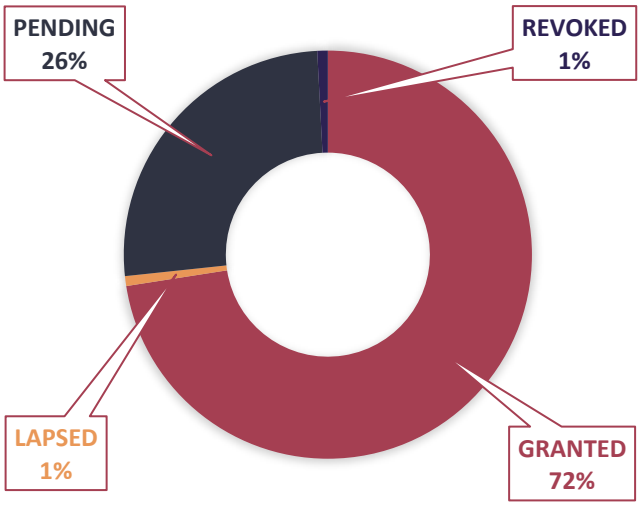
"3D NAND array is built with a gate-all-around (GAA) cell architecture. 3D NAND cells are ~20x larger in cell area and ~8x more electrons per 1V Vt shift compared to the scaled planar NAND cells (<20nm). This larger area results in improved reliability, improved Vt distribution and reduced interference."

- Micron

Since Jan 2018, around 2000 (1920+) patents have been published worldwide that relates to fabrication of monolithic 3D NAND memory. A distribution of patent shows that more than 500 patents are assigned to YMTC.

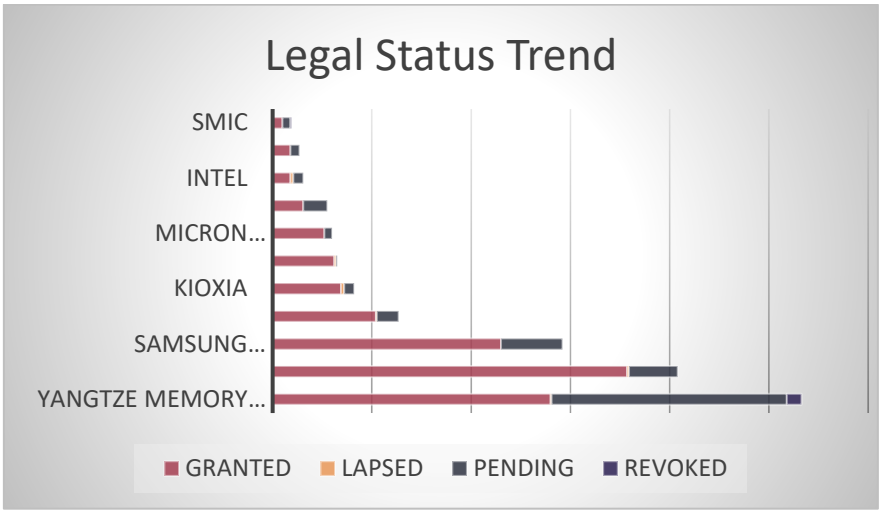


Since its inception, YMTC has invested heavily in R&D activities and has filed and obtained close to 4000+ patent in memory space. Interestingly, while considering the patents published since Jan 2018, YMTC has surpassed industry leaders in securing key technologies related to monolithic 3D NAND fabrication. While other fabricators do hold base technologies in this space, we anticipate they'd find it increasingly difficult to compete with YMTC.



Around 1/4th of the publications in this technology space are still pending which is a sign of healthy and actively growing technology. Out of these 1920 patents, a number of publications assigned to YMTC are still pending. A quick look at the patent pendency trend suggests that in coming years, YMTC will surpass the portfolio of SanDisk + Western Digital.

YMTC has hinted that in coming years, they have plans to monetize their intellectual property in this space by licensing out their proprietary monolithic 3D NAND fabrication technologies to players like Samsung and Micron.



YMTC has invested heavily in developing a strong patent portfolio in 3D monolithic fabrication space since its inception and it's quite evident from the rate of grant of patent on their technologies globally.

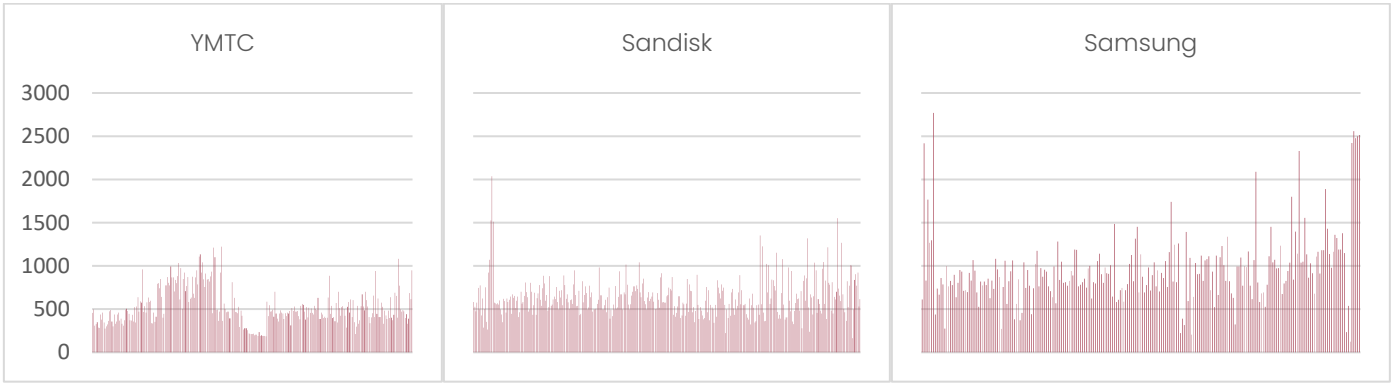
A quick look into the prosecution timeline of 3D NAND fabrication-related patents granted to the top 3 patent holding entities since Jan 2018 suggests that YMTC has obtained most of its patent rights in less than 500 days, either due to strong innovation or due to China's patent policy. While the average grant time for SanDisk® corresponds with USPTO standard timeline with an average prosecution time of 2 years, it seems like Samsung Electronics is yet to fine-tune its patent prosecution strategy in 3D NAND fabrication.

About YMTC

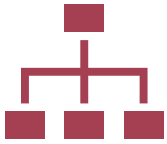
YMTC was established in Wuhan, China in July 2016. It is an IDM memory company focusing on the design, production, and sales of 3D NAND flash memory. YMTC provides 3D NAND wafer, die, and solutions.

In October 2017, YMTC successfully designed and manufactured China's first 3D NAND flash memory by combining independent R&D and international cooperation.

In September 2019, 64-layer TLC 3D NAND flash memory with innovative Xtacking® architecture was officially put into mass-production. In April 2020, YMTC announced its 128-layer 1.33Tb QLC 3D NAND flash memory chip, X2-6070.



3D NAND FABRICATION



Type of NAND Fabrication method

- Die Stacking
- Monolithic Fabrication

Why monolithic?

- Scalability
- High density

Key monolithic NAND Fabrication Steps

- Wafer Preparation
- Alternate Stack deposition
- HAR Etching
- Contact Pad formation
- Peripheral logic

3D NAND can be fabricated using two different approach of fabrication technique:

1. TSV or Die stacking or Chip Stacking where device wafers are processed and finished separately and are vertically connected at chip level with Through Silicon Vias.
2. In case of Monolithic 3D fabrication technique, a base wafer is prepared, and multiple layers of crystallized semiconductor material and metal layers are deposited using traditional fabrication methods. Monolithic 3D NAND is monolithically stacked single crystal silicon double-gated NAND flash memory where lithography steps are shared among multiple memory layers to reduce bit cost.

WHY MONOLITHIC 3D NAND?

1. 4X the density of conventional NAND flash.
2. Multiple generations of cost-per-bit improvement for same equipment cost and process node by using the same fab for multiple generations.

For fabrication of Monolithic 3D memory, each company has its own 3D NAND architecture, which are slightly different from one another. Samsung's technology is called Terabit Cell Array Transistor (TCAT), the Kioxia + Western Digital duo uses the term Bit Cost Scalable (BiCS) while YMTC uses its proprietary Xtacking architecture.

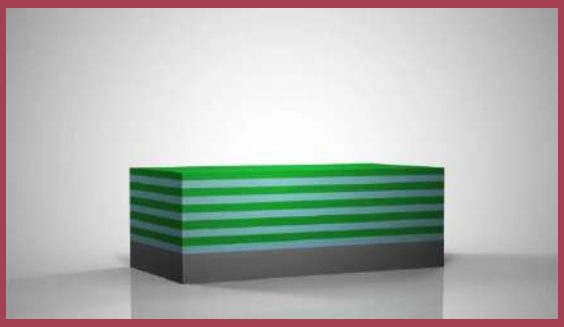
NAND Technology	YMTC 128L Xtacking	Samsung 128L V-NAND	Micron 128L CuA CTF	SK Hynix 128L 4D PUC
Device	Asgard AN4 1TB	Samsung EVO 870 1TB	Crucial BX500 480GB	SK Hynix Gold P31 1TB
Capacity per die	512 Gb	512 Gb	512 Gb	512 Gb
Die size	60.42 sq. mm	74.09 sq. mm	66.02 sq. mm	63 sq. mm
Memory density	8.48 Gb per sq. mm	6.91 Gb per sq. mm	7.76 Gb per sq. mm	8.13 Gb per sq. mm

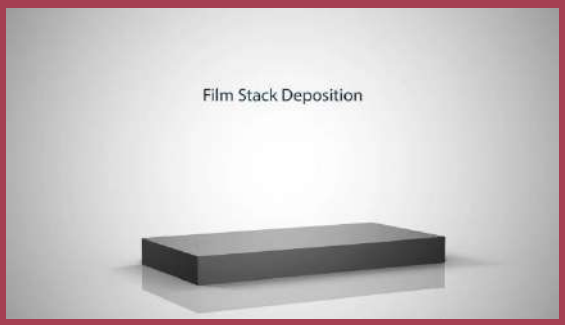
Data Source: Tech Insights

Though each company has developed their own fabrication method, a generic flow of Monolithic 3D NAND fabrication process as explained by LAM Research can be summarized as:

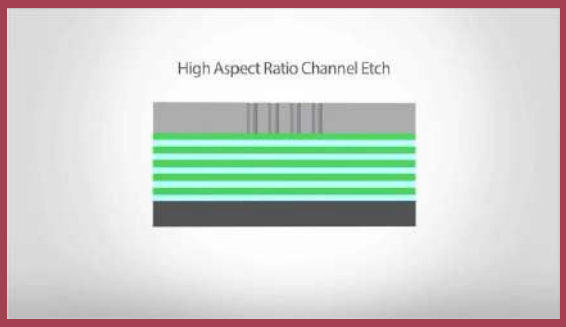
STEP 1

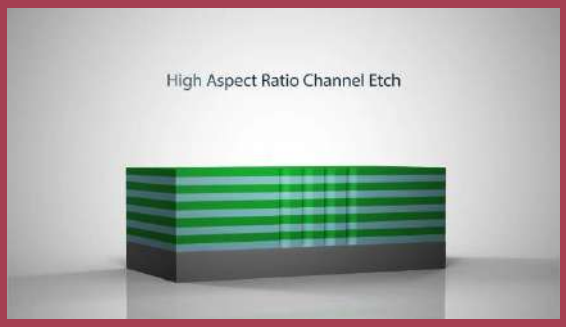
Using chemical vapor deposition (CVD), alternating thin layers are stacked on the substrate. Each company uses a different set of materials to create a stack of layers generally alternating oxide and nitride films. For example, in Samsung's 3D NAND technology, the company deposits alternating layers of silicon nitride and silicon dioxide on the substrate.





The next step, HAR etch is toughest. Etching tool drill tiny circular channels from the top of the device stack to the bottom substrate. The channels enable the cells to connect with one another in the vertical stack. In this process, a carbon-based material is first deposited on the stack. That material becomes a hard mask. The next step is to pattern holes on the top of the hard mask.

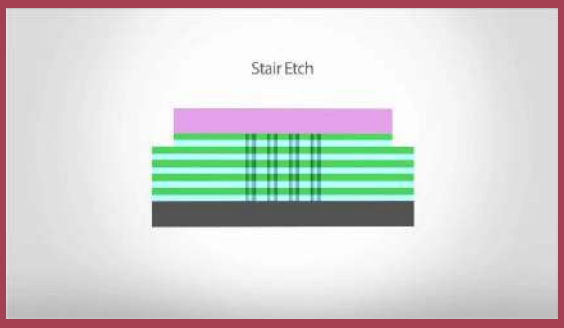


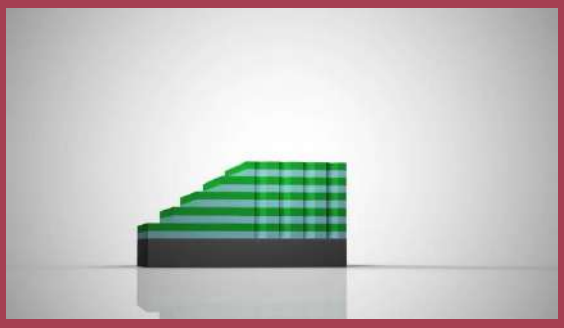


STEP 2

STEP 3

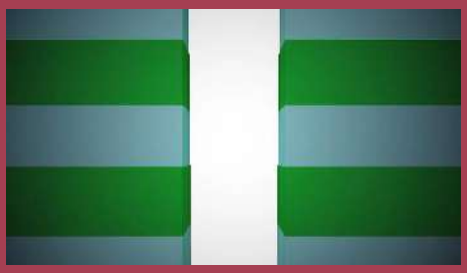
Contact pads to the word lines are created using controlled etches that produces distinctive staircase shape



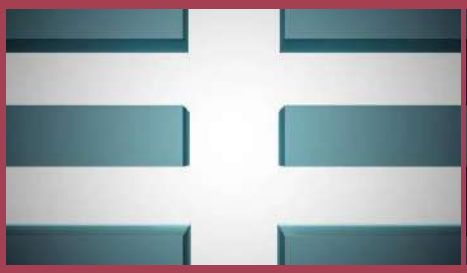


While Samsung fills the remaining gaps in the structure with the tantalum nitride control gate material. The resulting structure is a vertical NAND string of TANOS (tantalum-alumina-nitride-oxide-silicon) transistors.

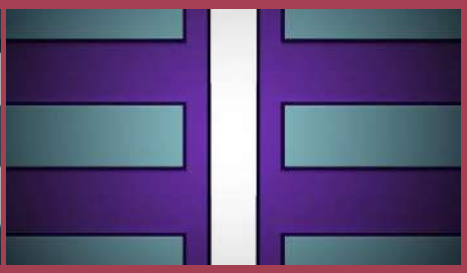
A few of the memory manufacturers remove the nitride layers and fill a tungsten conductive metal gate material to create tungsten word lines by atomic layer deposition process.



Alternating Nitride Layers

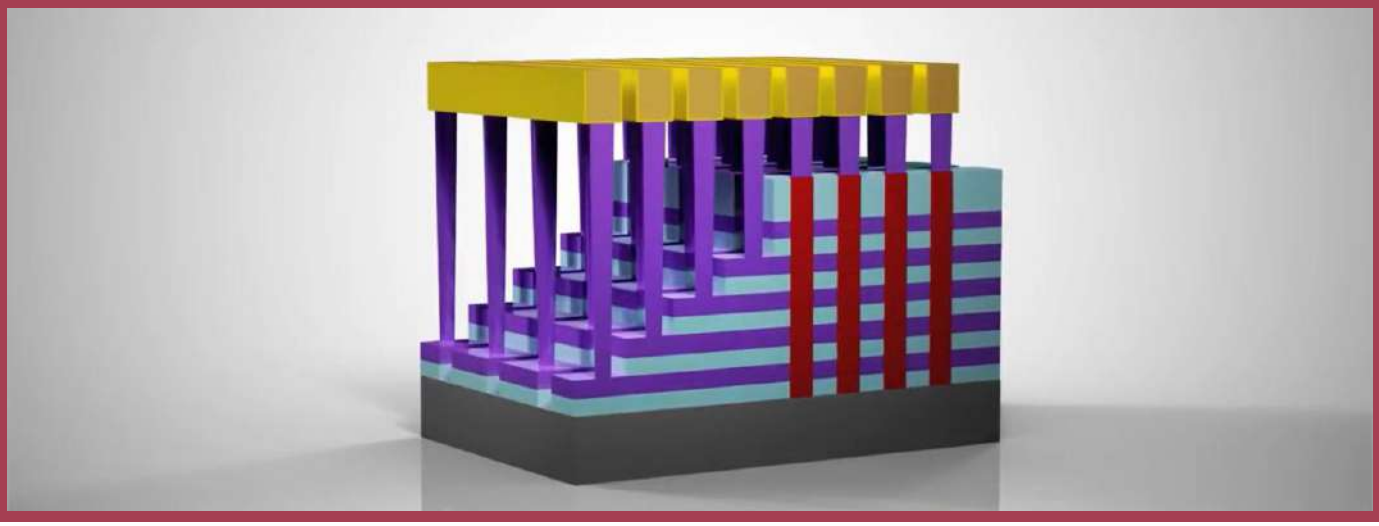


Nitride Layers removed



Tungsten fill

Finally, the peripheral logic is connected to the control gates.



STEP 4

PATENTING TRENDS

Patenting Trend

- Publication Trend
- Innovation trend

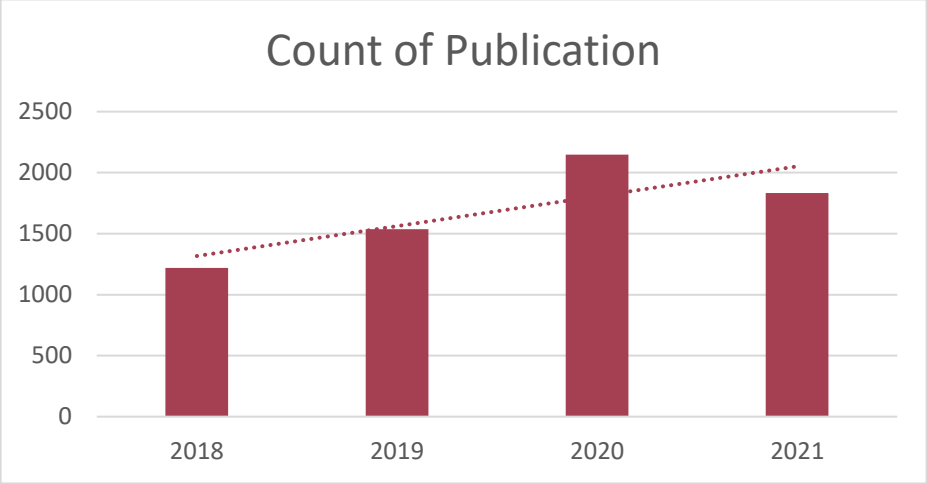
- MOSFET memory technologies
- Floating Gate
- Charge Trap
- Key patenting trends since Jan 2018

Fabrication Equipment

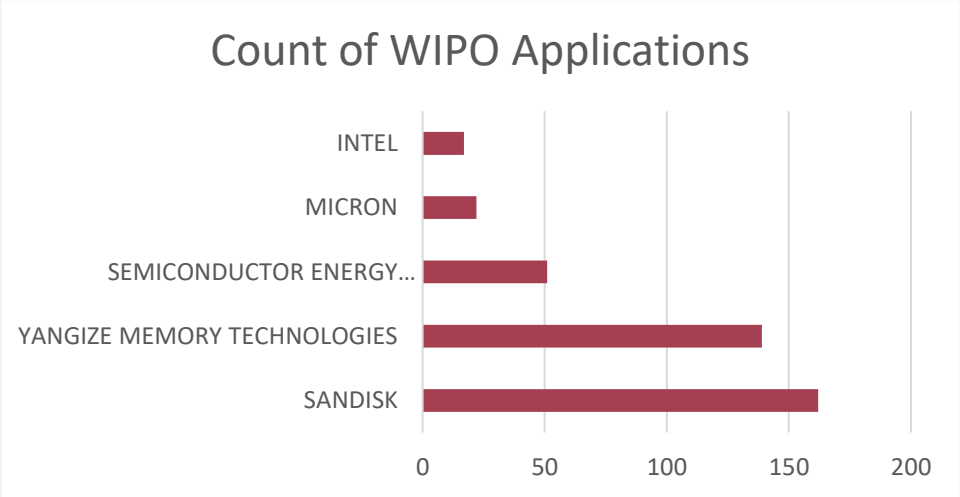
- Key players
- Patent and market distribution

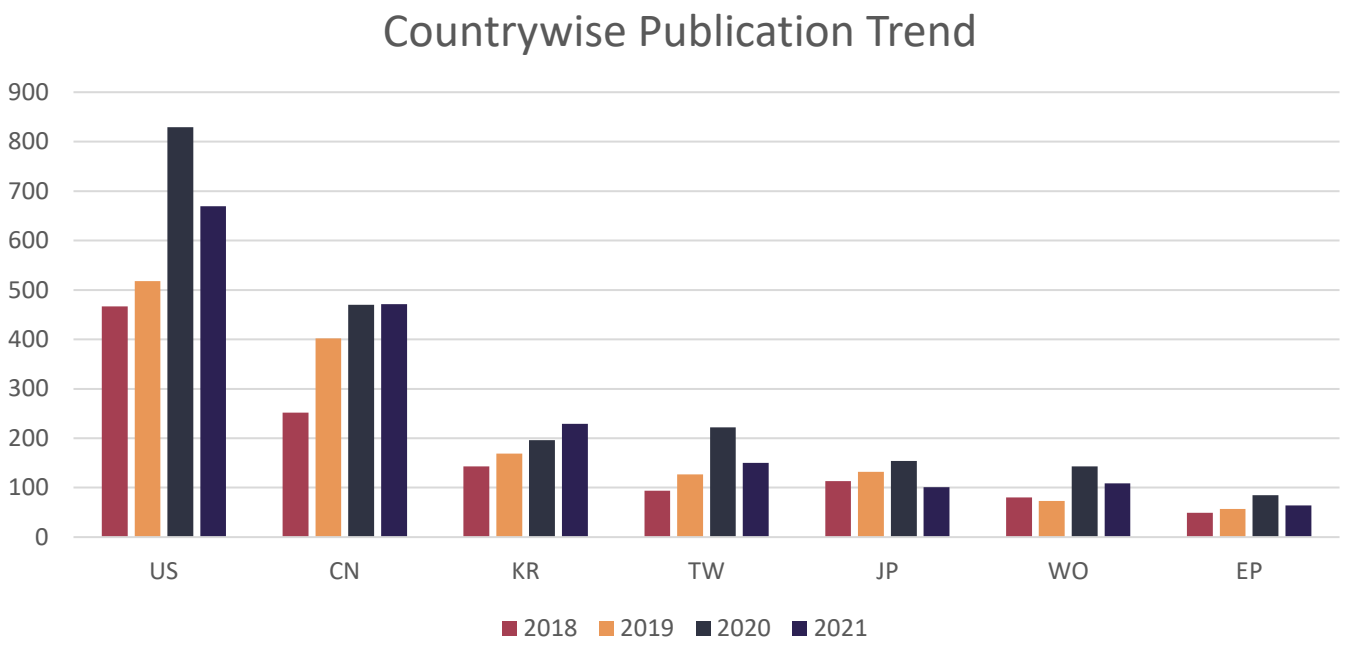
PUBLICATION TREND

More than 6500+ individual patent application spread across 1900+ patent families have been published since Jan 2018. With more than 33% Patent publications, US is leading the 3D NAND Fabrication technology race. However, post 2019, a sudden surge in patent publication was observed in China which is primarily due to patent filings by YMTC.



Out of these 1920+ publications, around 475 publications correspond to WIPO applications. Interestingly, Samsung hasn't shown much interest in WIPO route rather preferring the traditional Paris Convention route to file patent applications in memory markets like Korea, US, China, and a handful of European countries.

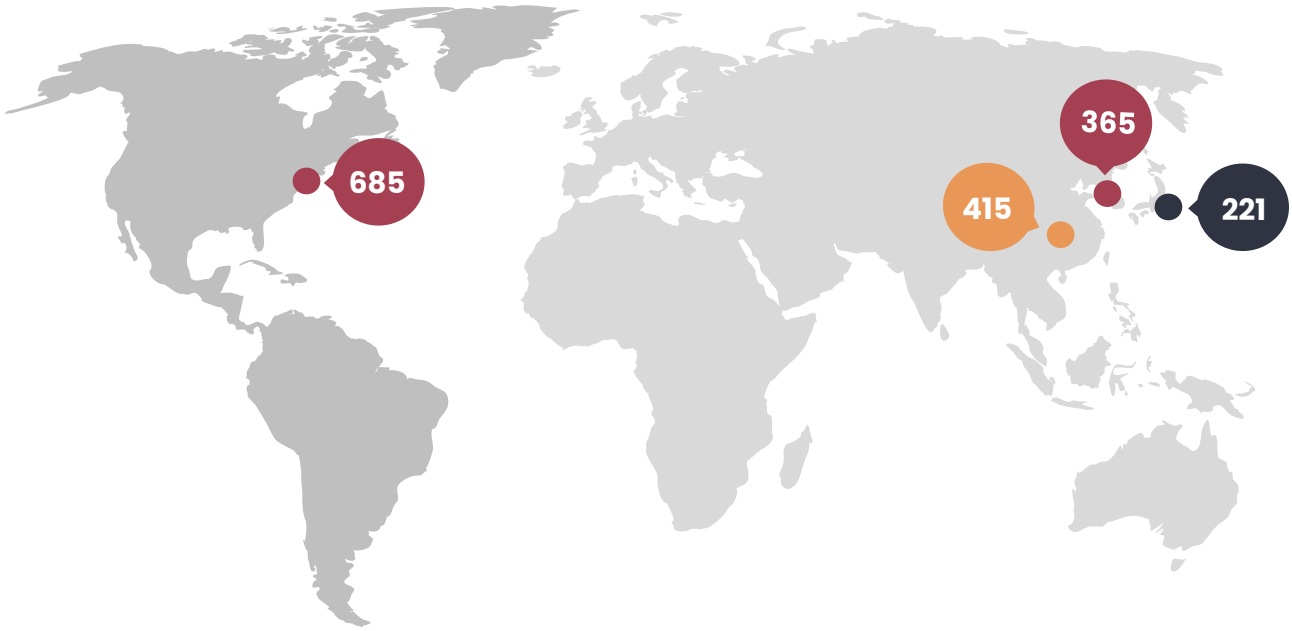




Most of the technologies filed in the USA and China with Sandisk and YMTC being the key technological players in respective jurisdictions. Followed by South Korea where majority of the patents are filed by Samsung and SK Hynix.

ORIGINATION TREND

Approximately 1/3rd of the Monolithic 3D NAND fabrication related patents published since Jan 2018 originated in the US with SanDisk, Micron & Intel being the topmost entities while Samsung & SK Hynix have their 3D NAND fabrication research based out of South Korea. Though China was lagging till 2018, they have swiftly accelerated after YMTC entered the play, which holds approximately 40% of the patents published in the space since Jan 2018.

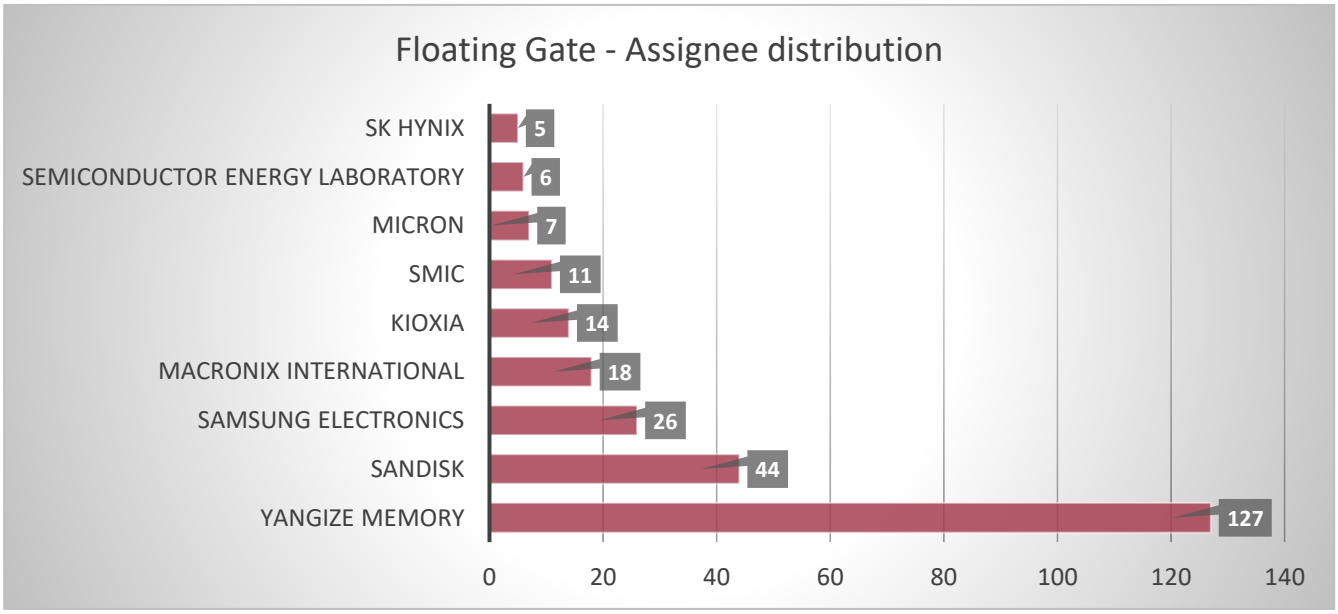


FLOATING GATE & CHARGE TRAP

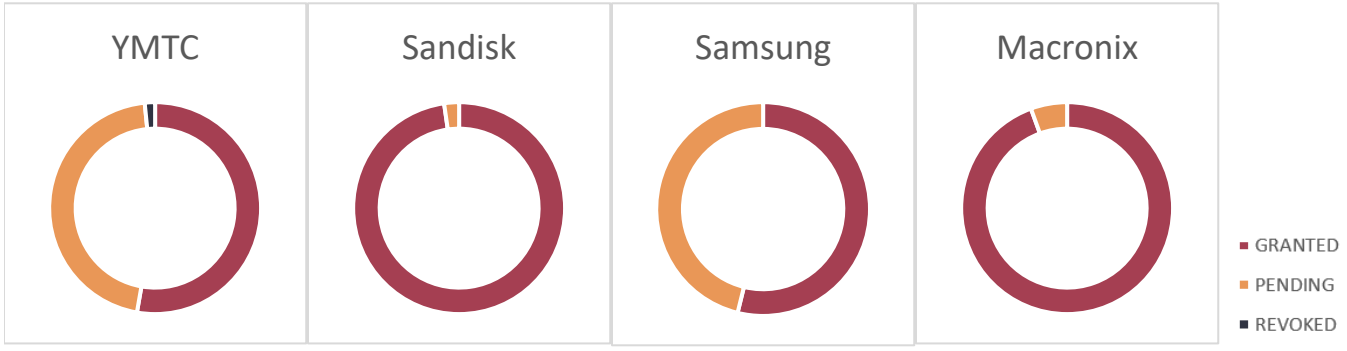
FLOATING GATE TECHNOLOGY

Traditionally, SSD uses floating gate cells where each cell contains one floating gate that's integrated into the cell's structure. The floating gate traps and releases electrons by application of voltages at different levels.

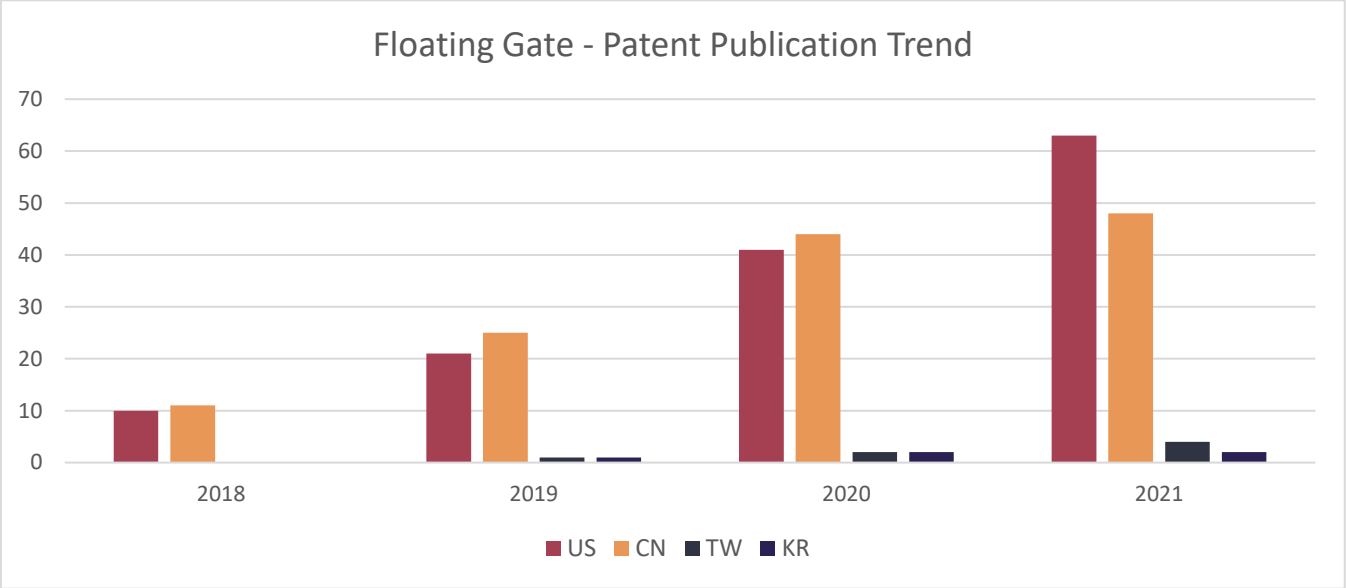
An oxide layer separates the floating gate from the silicon substrate. The oxide layer is thin enough for electrons to pass between the floating gate and substrate when voltage is applied during a programming, read, or write operation. A quick analysis of patents published after Jan 2018 indicate that most of patents that explicitly claim technologies pertaining to Floating gate type 3D NAND fabrication are assigned to YMTC followed by SanDisk and Samsung.



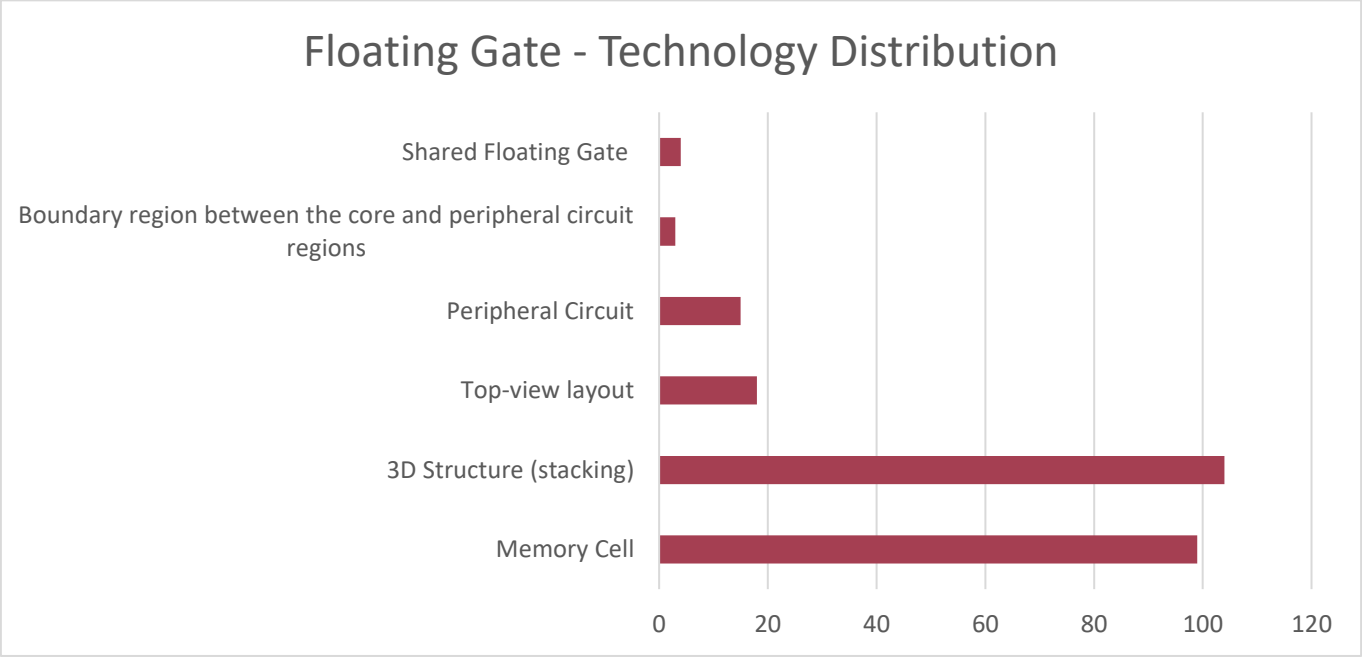
Legal status of these patents suggest that a lot of YMTC's patent applications in this space are still pending and will help position YMTC at the top spot in coming days.



Traditionally, Intel and Micron use Floating Gate based technology for their memory devices. However, due to faster programming and write operations, nowadays, Charge Trap based 3D NAND memory devices are preferred by most memory fabricators. Although, Charge Trap is one of the technological strengths of YMTC, yet we have seen a steep growth in patent count over the last couple of years that relates to Floating Gate type 3D NAND memory fabrication, most of which are assigned to YMTC.



The patents in the 3D NAND memory mostly claims 3D stacking methods and arrangements followed by memory cell arrangements. Among the scope of the claims (see chart below), a lesser number of patents discusses/claims about area/scope between the core and peripheral circuit regions. Also, it is notable that the below differentiated methods are mostly claimed as combinations. There are a good number of patents claiming about the gate arrangements.

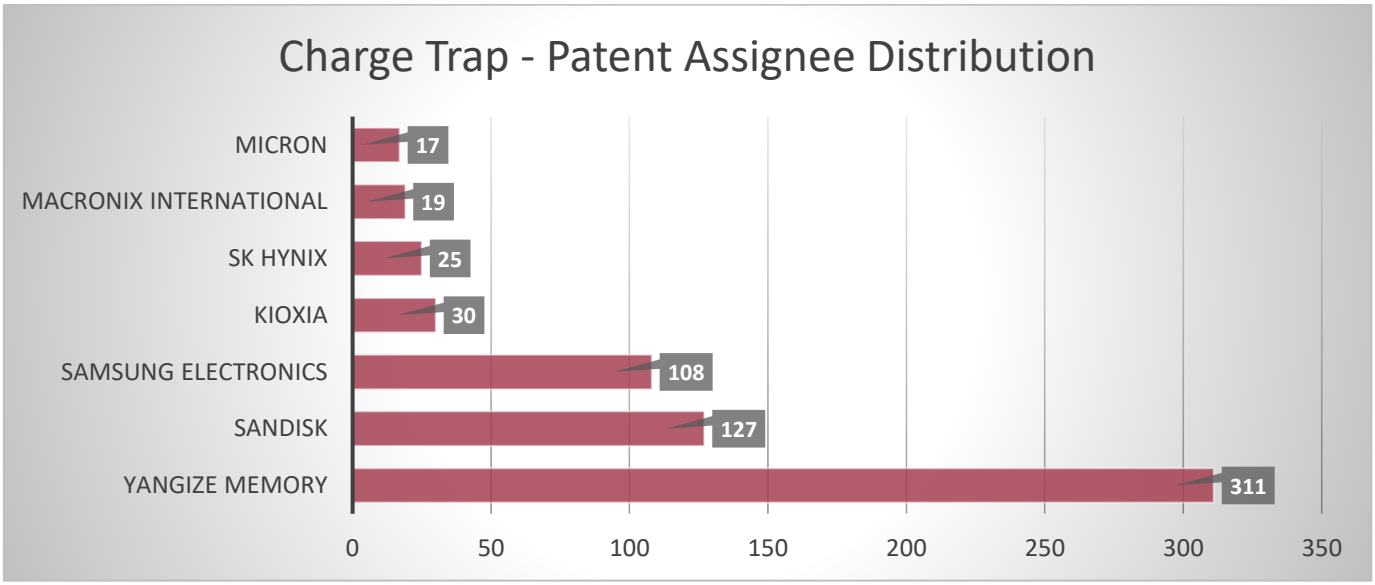


CHARGE TRAP TECHNOLOGY

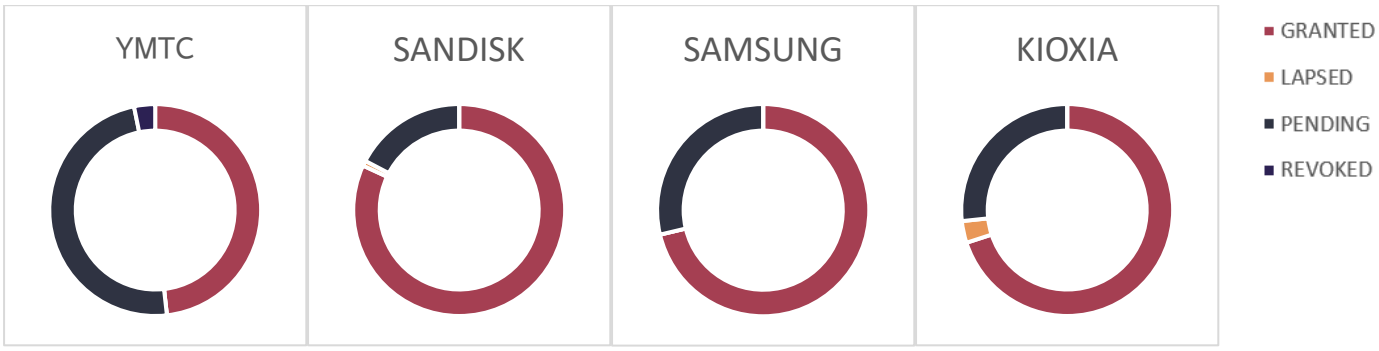
On the other hand, Charge Trap cells work much like floating gate cells, with different voltage patterns to move charge into and out of a trapping layer. Floating gate uses polycrystalline silicon to provide a conductor for trapping the electrons while the charge trap uses silicon nitride to provide an insulator. To sum up, Charge Trap cells are advantageous over floating gates in many ways.

As floating gate cells become smaller, they also become more susceptible to disruptions, such as electrons inadvertently flowing from one floating gate to another.

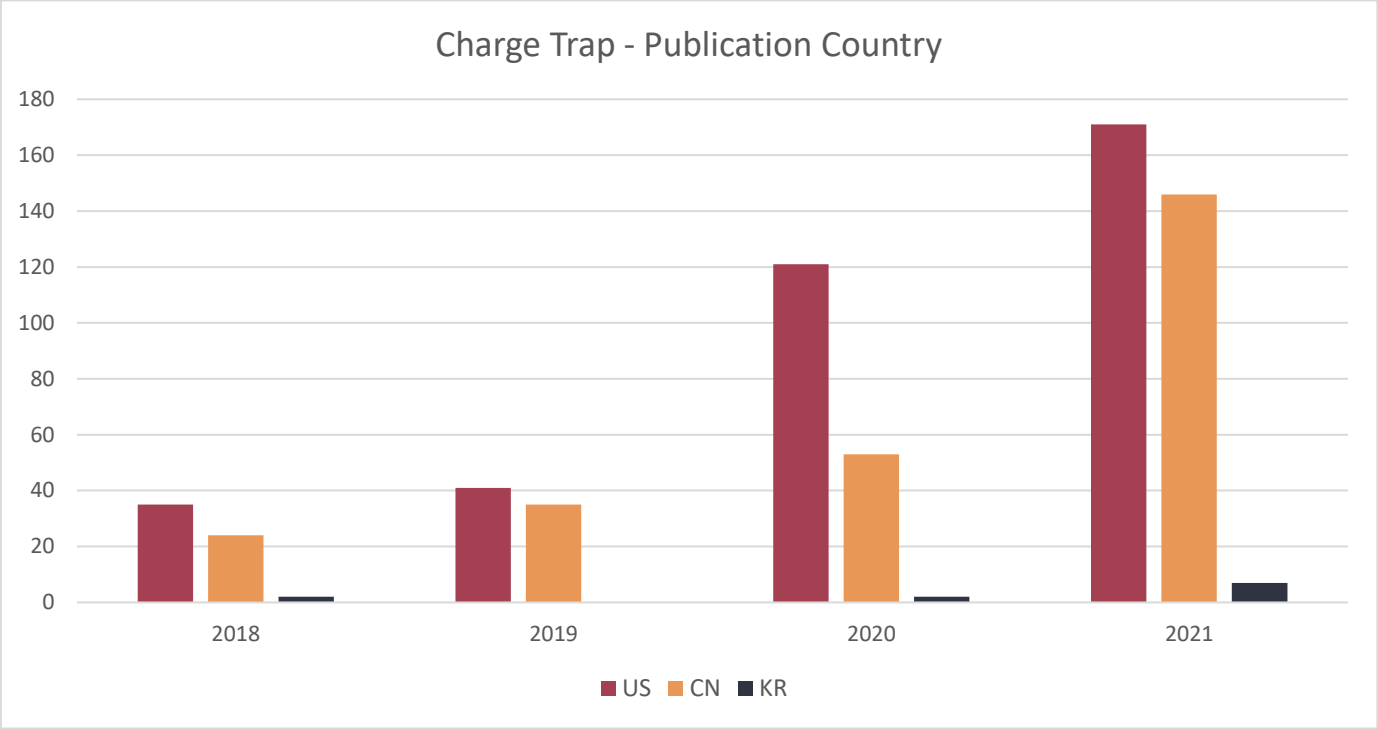
Since Jan 2018, YMTC has secured more than 310 patents that directly relates to innovations in Charge Trap type 3D NAND Memory fabrication. SanDisk, its closest competitor, has published more than 125. The year-to-year gap in patent filings between YMTC and SanDisk (and others) in this space is only widening over the last three years, and it seems like SanDisk and other competitors of YMTC may need to come out with a better technology plan.



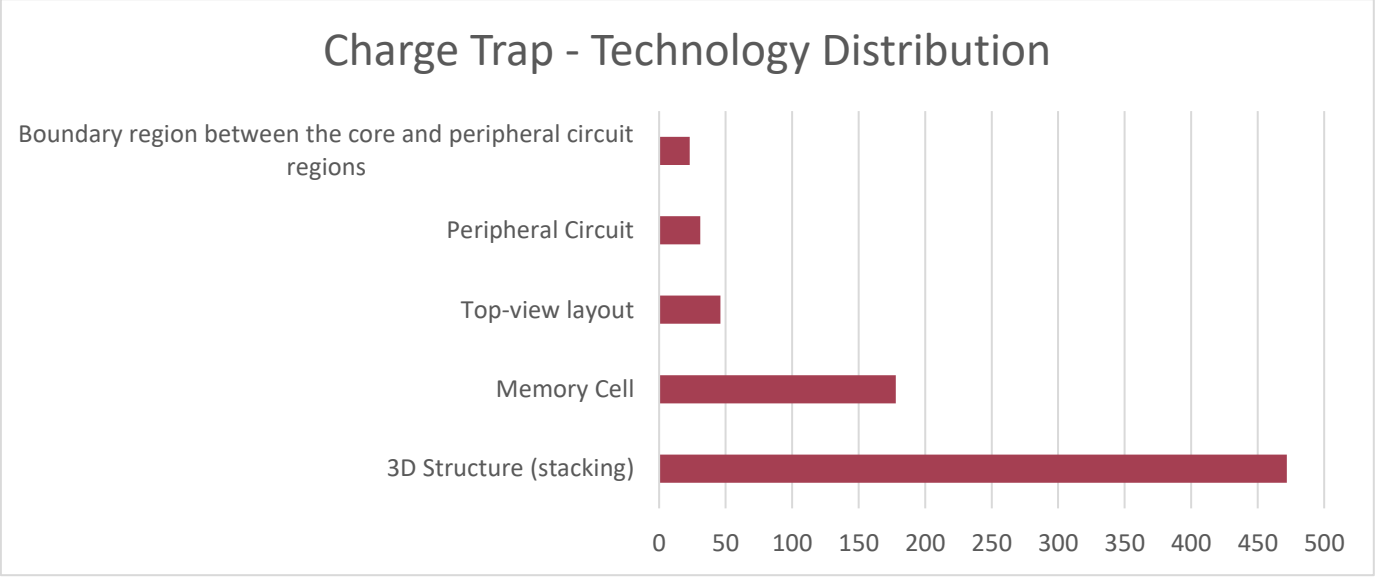
Legal status of these published patent applications indicates that close to 50% of the patent families published by YMTC is in still pending which suggest that the base technology on which YMTC is working isn't saturated yet and therefore, we should expect to see a lot newer improvements/ continuation patents being filed in the coming days.



Most of the patents teach different aspects of charge trap based fabrication and of these, most have been filed in US and China with a few filed in Korea, Japan, and a few European countries. YMTC is a key entity from China and Micron & SanDisk from the USA. Most of the patents filed by Samsung relates to generic fabrication process not specific to any MOSFET type.

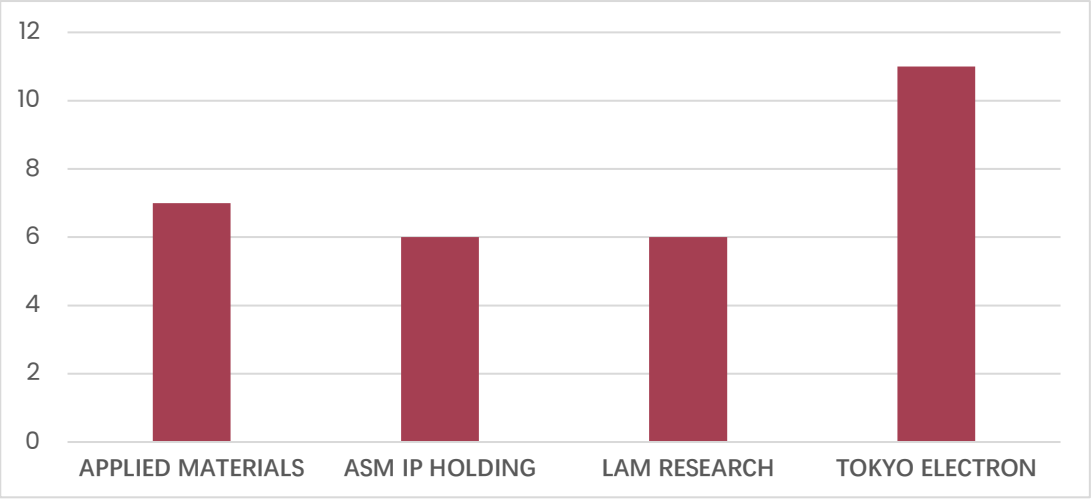


Most of the patents pertaining to charge trap based 3D NAND memory fabrication technology relates to different aspects of 3D stacking methods viz, staircase structure, 3D arrangement of layers and the like, followed by memory cell arrangements. In comparison, very few patents cover technologies that relates to peripheral circuits and their interconnection with memory core region. Also, it is noteworthy that the below differentiated methods are mostly claimed as combinations.



FABRICATION EQUIPMENT

Apart from the normal fabrication equipment, NAND fabrication requires specialized equipment for fabricating channel, etching and metal deposition where non-line of sight metal is deposited. Primarily etching related equipment perform High Aspect Ratio (HAR) etching, hard-mask opening, resist trimming, conductor/dielectric etching while deposition related equipment deals with Plasma Enhanced (PE) CVD and ALD for dielectric and conducting materials deposition. Highly specialized tools are used for hybrid bonding/ wafer-to-wafer bonding such as YMTC's Xtacking™. Since Jan 2018, close to 30 publications are assigned to these top four equipment suppliers. These patents generally relate to innovations that are explicitly designed for 3D NAND fabrication like etching, wafer preparation etc.



Lam Research has introduced Vantex™, its latest in dielectric etch technology designed specifically for Sense.i™.

Applied material is focusing on further increasing capacity by reducing the size of each cell. Applied's innovative systems are helping Flash memory manufacturers scale this technology to 96 layers and beyond.

Starting in 2023, ASML plans to deliver the first batch of next-generation EUV equipment that will take the EUV numerical aperture (NA) higher than current machines are capable of, from 0.33 NA to 0.55 NA.

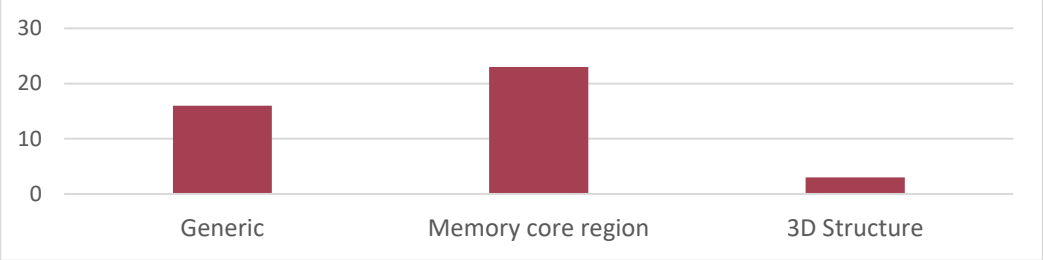
ASML, Applied Materials, Tokyo Electron and Lam Research hold more than 75% of the overall equipment market. While ASML leads the lithography related equipment, LAM research leads the etching division.

CHALLENGES IN 3D NAND FABRICATION

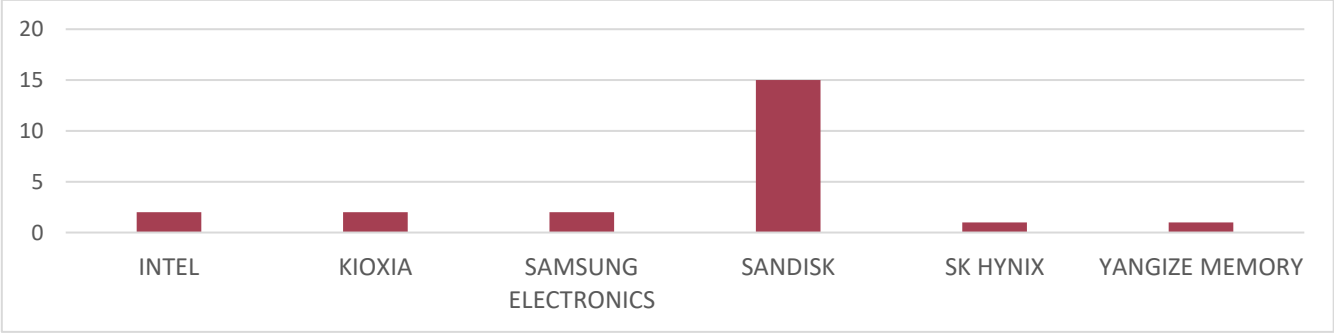
Etching & metal deposition are the biggest challenges in 3D NAND fabrication. Etching tools must drill deep channel holes from the top of the device to the bottom substrate. While deposition tools must produce high-quality defect-free thin films with nanometer thicknesses. In recent years, inspection tools are also gaining popularity to monitor the processes and maintain high yields.

FERROELECTRIC NAND

NAND Flash memory devices presently use floating-gates or charge trap type NAND transistors that are based on electron-tunneling effect through a tunnel oxide. The electron-tunneling process requires voltage pulses with high amplitude and long duration; however, existing flash memory devices possess a high functional voltage approximating 20 volts and a slow speed coupled with limited endurance. To obtain fast functionality at a low power with fast switching capabilities, researchers are working on ferroelectric materials-based memory devices for commercial use. Since Jan 2018, more than 50+ patents have been published in this space that specifically relate to Ferroelectric based NAND.



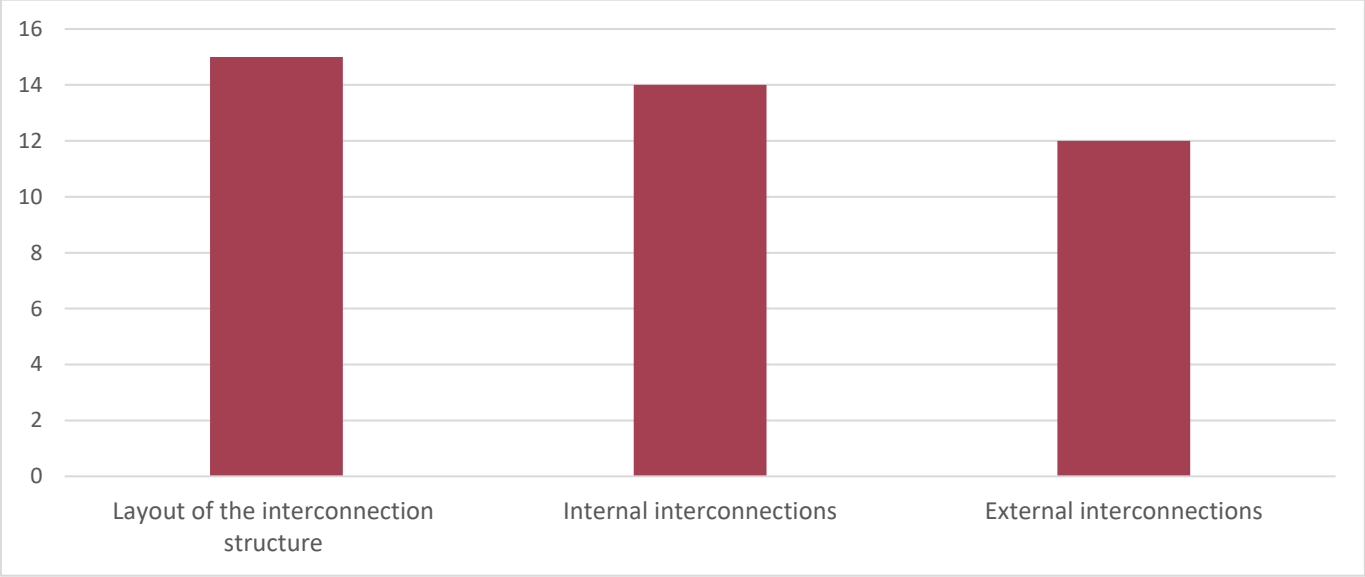
Although not widely discussed in forums and research journals, most of the patents that claim fabrication of NAND with a ferroelectric layer are assigned to SanDisk.



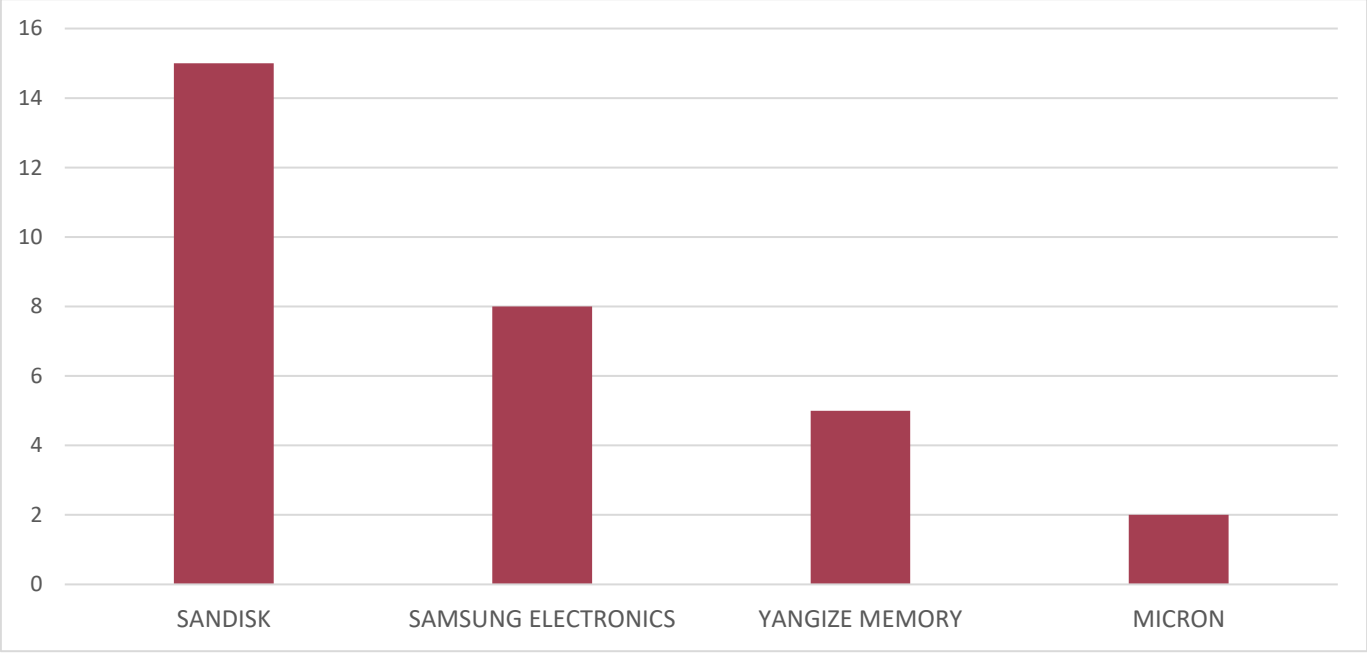
METAL DEPOSITION AND INTERCONNECTS

Once the gate is developed, the device requires contacts. The device is backfilled with a conductor using a metal deposition step which itself is a challenging task. It's a tricky task, that involves a non-line-of-sight deposition of conductive material.

Apart from the generic interconnection related patents, around 40+ patent publications relate to core aspect of interconnections and contact formation for monolithic 3D NAND memories. Out of which the prime focus is to tackle the challenging out-of-line deposition.



Patent data of the last 3 years suggests that companies like SanDisk and Samsung are focusing these problems and spending good amount of R&D expenses in this area.



TECHNOLOGY LEADERS

"We are building a new company!"

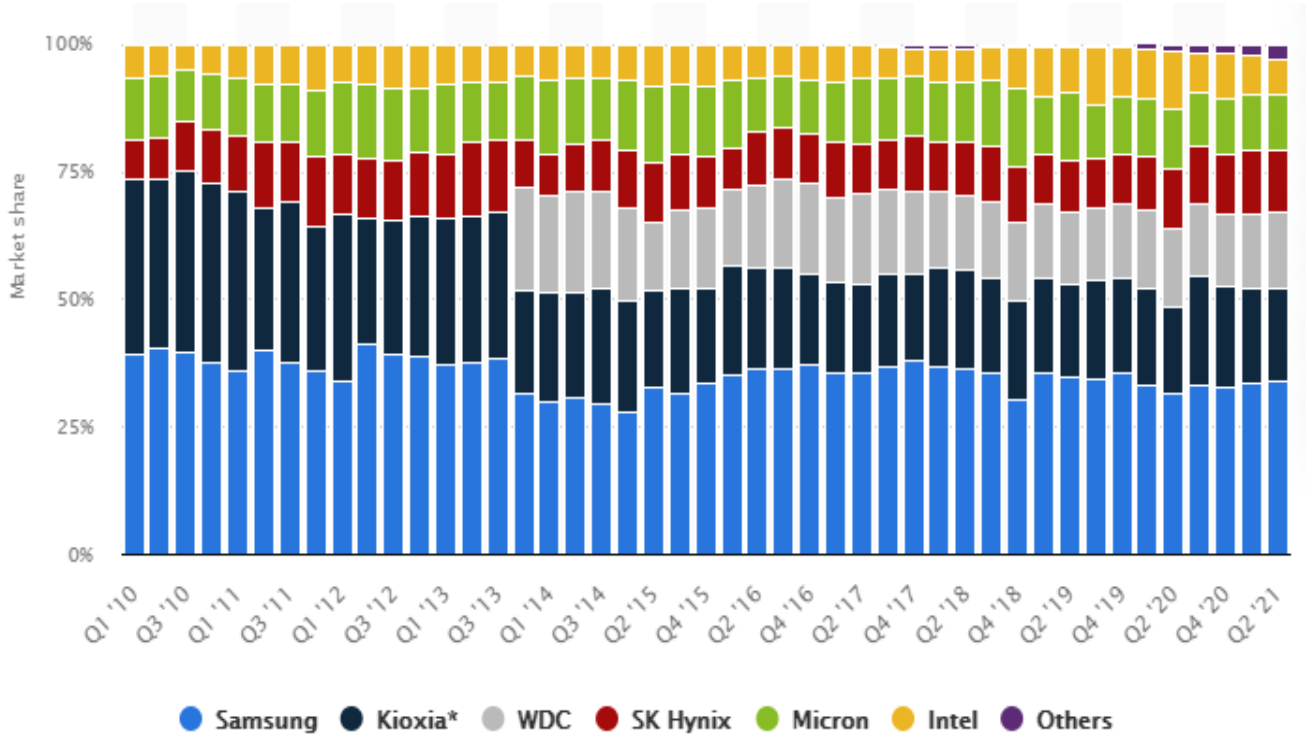
Robert Crooke,
Senior VP & GM
Intel's NAND Products

WORLDWIDE REVENUE SHARE

So far Samsung is undoubtedly market leader in the NAND memory market segment. As per data released by Statistica.org, Samsung caters to more than 1/3rd of memory supplies, followed by Kioxia, Western Digital, SK Hynix, Micron, and Intel. However, due to recent mergers and collaborations and entry of new players in the market, more specifically YMTC - the market dynamics are bound to change in the coming years.

Though Kioxia and Western digital claim to possess a healthy partnership, there are news that Western Digital has plans to acquire Kioxia for the substantial sum. Also in 2018, the cessation of the Intel and Micron partnership for 3D NAND memory was a major change. Very recently, SK Hynix purchased Intel's NAND business and now have plans to turn Intel NAND business into a stand-alone US Company.

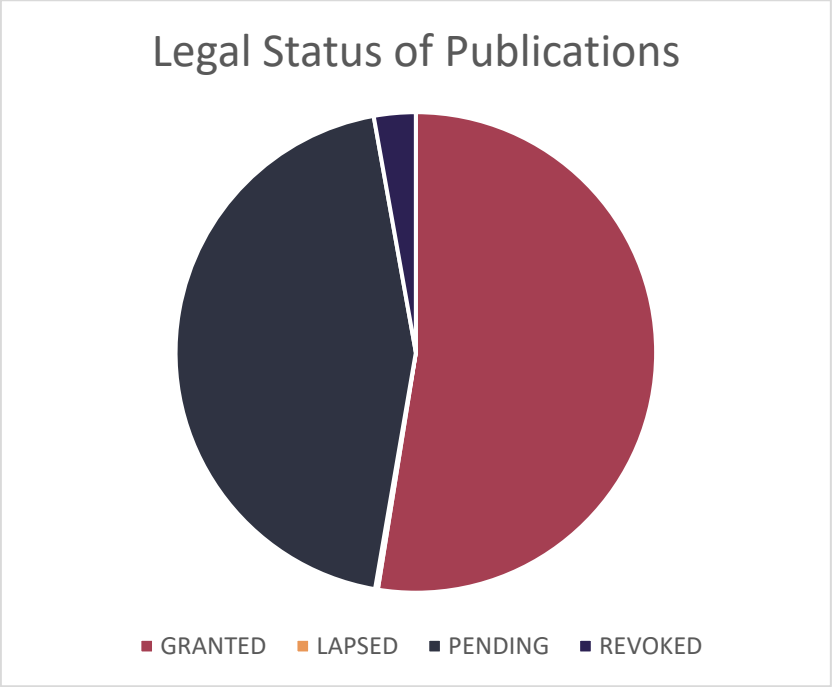
Technologically, every company is keen to obtain more and more patents in this lucrative and futuristic monolithic 3D NAND memory segment and are constantly coming up with technologies to scale the memory density and provide a robust architecture.



YANGTZE MEMORY

In the past few years, YMTC has focused on all aspect of 3D NAND fabrication including wafer preparation, stacking, interconnection of peripheral logic and everything in between.

YMTC is not only securing fresh patents in 3D NAND fabrication space but also licensing-in best technologies. Recently, YMTC has obtained access to a foundational portfolio of Xperi's DBI hybrid bonding technology.



A closer look into legal status of patents assigned to YMTC suggest that more than 40% of the patents assigned to TMTC are still pending and a lot more continuation patents are expected in the coming years.

Recent patenting trend suggest that YMTC is investing in layer stacking technologies along with a new improved architecture for NAND memory.

Recent Patents:

CN113451319
CN113421834
CN113410251
CN113451326
CN113410250

Most of YMTC's recent patent publications claim about stacking of layers/substrates. In particular, they teach formation of stacks using a pair of isolation structures or a set of layers/substrates. Also, these recent research works focus on the advantage of compact size and cost cutting.

Recent Patents

KR10-2021-0104607
KR10-2021-0066763
KR10-2021-0053824
KR10-2021-0037629
KR10-2021-0030306

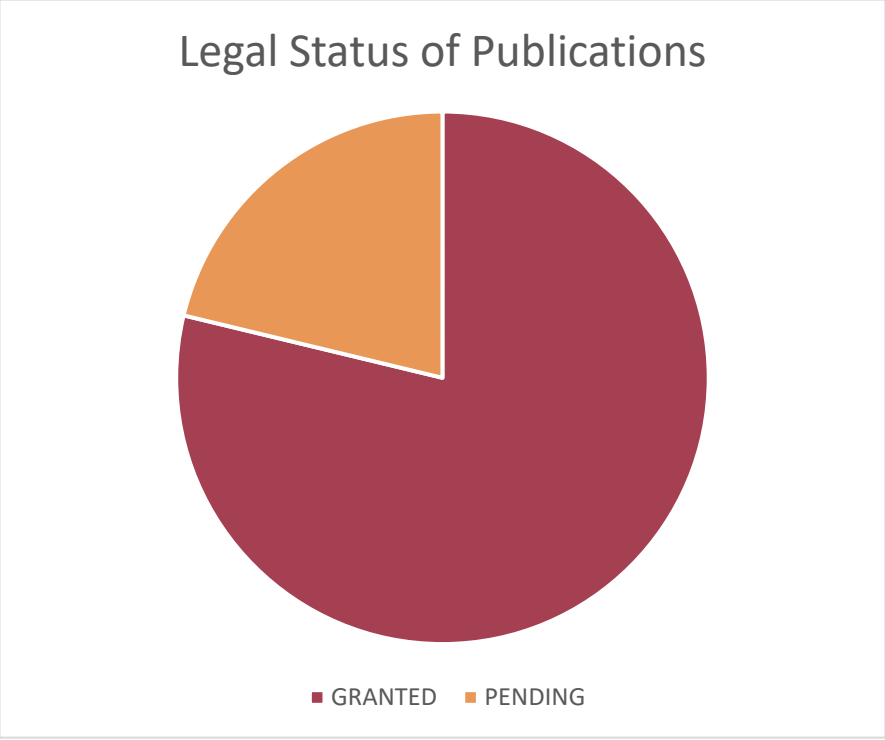
Most of Samsung's recent patent publications relate to improved production, yield, performance, and reliability.

Few of the recent patents relate to 3D NAND memory devices capable of improving performance by using a charge storage layer including a ferroelectric material. While others relate to memory devices capable of more uniformly controlling characteristics of stacked memory cells and stacked structure; and induces self-alignment and prevents bursting of the contact structure.

SAMSUNG

Samsung is the undisputed leader in the memory market segment and like its other memory technologies, Samsung is investing significantly in its vertical NAND (V-NAND) technology. Most of their patents in this technology space relates to charge trap technology. In 2013, the first V-NAND solution developed by Samsung featured 24 layers, which has now evolved to almost 200 layers, a number that continues to grow.

However, much like with high-rise apartments, simply stacking more layers on top of one another is not everything. Samsung managed to reduce the cell volume by up to 35% by decreasing both its surface area and height through highly innovative 3D scaling technology. Though Samsung holds a good count of patent in this domain, yet the legal status suggests that most of their patented technologies are at the verge of saturation, and they need to come out with more innovative ways to maintain their position.

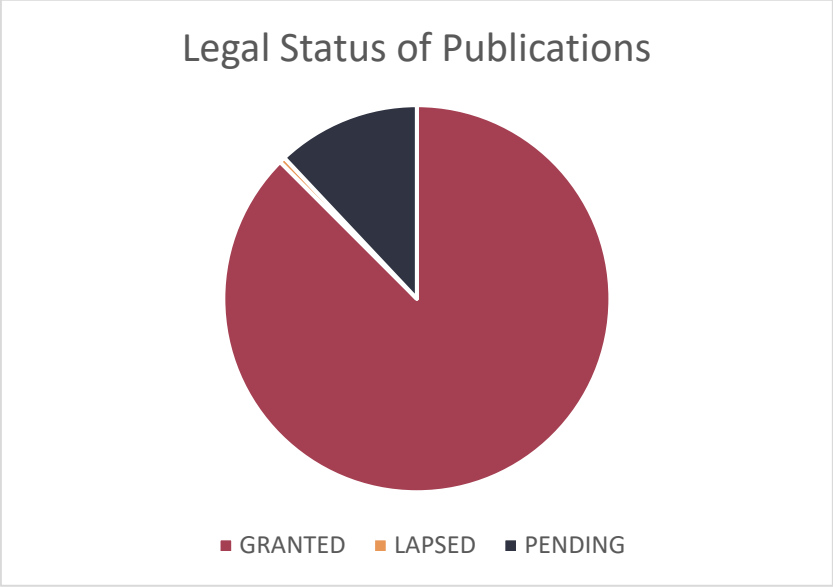


WESTERN DIGITAL

After acquisition of SanDisk in 2015, Western Digital as an entity has shown more interest in communication part (read, write and related operations). SanDisk is spearheading their 3D NAND memory fabrication segment which is reflected from the fact that most of the innovations are assigned to SanDisk.

Earlier this year, Kioxia Corporation and Western Digital announced their sixth-generation, 162-layer 3D flash memory technology and stated that the duo is working on a new approach to 3D flash memory scaling. With this new generation innovation, Kioxia and Western Digital are introducing innovations in vertical as well as lateral scaling to achieve greater capacity in a smaller die with fewer layers.

In the last couple of years, SanDisk has acquired lot of commercially valuable technologies in the space and has plans to give tough competition to its traditional rivals and YMTC with its innovative technologies.



Recent Patents

US11069410
US11043266
US11081190
US20210304822
US20210305266

Very recently, SanDisk has acquired patent rights on a three-dimensional NOR-NAND combination memory device.

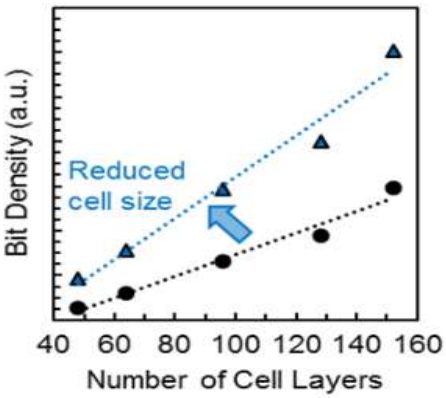
"*Through our strong partnership that has spanned two decades, Kioxia and Western Digital have successfully created unrivaled capabilities in manufacturing and R&D. Together, we produce over 30 percent1 of the world's flash memory bits and are steadfast in our mission to provide exceptional capacity, performance and reliability at a compelling cost.*"

Masaki Momodomi
CTO, Kioxia

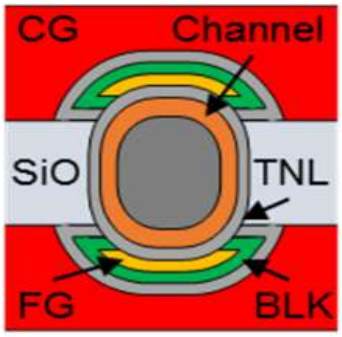
WHAT'S NEXT

Kioxia and Western Digital has recently announced that the companies have developed their sixth-generation, 162-layer 3D flash memory technology based on a new split-gate architecture. The new device will likely stack two 80-layer structures on top of each other, forming a 160-layer device.

In split-gate, circular-shaped control gates are formed, which are then split into two smaller semi-circular gates. By splitting the gate into two parts, the cell size is reduced by half, thereby increasing the capacity.



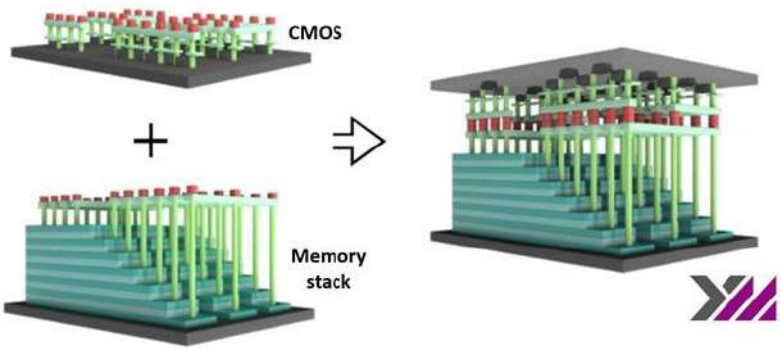
(a)



(b)

Global storage leader Samsung has moved their R&D onto the 8th generation V-NAND platform by stacking 200 layers or above. On the other hand Micron has recently announced their new 3D flash memory technology, which has 176 layers of memory cells stacked on top of each other.

YMTC takes a different approach than others. It processes the periphery circuits and memory array on two separate wafers. Then, it stacks and joins them using a copper hybrid bonding technique. The periphery circuits are above the memory, enabling higher bit density. But this bonding technique is still expensive. YMTC is actively working on different aspects to make it cost effective.



YMTC has already started the production of 128-Layer, 3D QLC NAND memory and has plans to transition to its Xtacking 3.0 design sometime in the latter half of 2022, with production capacity expected to reach its peak output by then. Based on the recent technological advancements and patent data analytics, it seems like YMTC is poised to lead in NAND Flash Technology space. As per former chairman of YMTC, the company aims to lead competitors like Samsung and Micron in NAND flash technology and will very likely license its knowhow to rivals in the next few years.

CHALLENGES FOR MEMORY MANUFACTURERS

The 3D NAND market remains dynamic with various fast-changing trends and events taking place in the arena. Prime drivers among them would be:

- **More stacking.** The ability to stack all 3D NAND layers on the same die is running out of steam, forcing some to take new stacking approaches.
- **New architectures.** Vendors are developing new gate and die schemes to enable faster and smaller chips.

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